WHAT IS CLAIMED IS:

1. An operational amplifier circuit, comprising:

a first inverted amplifier circuit that receives a first input signal;

a second inverted amplifier circuit that receives a second input signal;

a third inverted amplifier circuit that receives an estimated common-mode output signal and an output signal of said first inverted amplifier circuit and outputs a first output signal and a second output signal;

a fourth inverted amplifier circuit that receives the estimated common-mode output signal and an output signal of said second inverted amplifier circuit and outputs a third output signal and a fourth output signal;

a first non-inverted amplifier circuit that receives the estimated common-mode output signal and outputs an output signal, the output signal of the first non-inverted amplifier circuit fed back to the output signal of the first inverted amplifier circuit; and

a second non-inverted amplifier circuit that receives the estimated common-mode output signal and outputs an output signal, the output signal of the second non-inverted amplifier circuit fed back to the output signal of the second inverted amplifier circuit,

wherein adding the second output signal and the fourth output signal generates the estimated common-mode output signal.

2. The operational amplifier circuit according to claim 1, wherein the first and second input signals are differential input signals.

3. The operational amplifier circuit according to claim 1, further comprising:

a fifth inverted amplifier circuit that receives an output signal of the first inverted amplifier circuit and outputs an output signal that is fed back to the output of the first inverted amplifier circuit;

a sixth inverted amplifier circuit that receives an output signal of the second inverted amplifier circuit and outputs an output signal that is fed back to the output of the second inverted amplifier circuit;

a seventh inverted amplifier circuit that receives an output

signal of the first inverted amplifier circuit and outputs an output signal that is fed back to the output of the second inverted amplifier circuit; and

an eighth inverted amplifier circuit that receives an output signal of the second inverted amplifier circuit and outputs an output signal that is fed back to the output of the first inverted amplifier circuit.

4. An operational amplifier circuit, comprising:

a first inverted amplifier circuit that receives a first input signal;

a second inverted amplifier circuit that receives a second input signal;

a first non-inverted amplifier circuit that receives a common-mode input signal,

a second non-inverted amplifier circuit that receives a common-mode input signal,

a third inverted amplifier circuit that receives an estimated common-mode output signal and a sum of the output signal of the first non-inverted amplifier and the output signal of the first inverted amplifier circuit, and outputs a first output signal and a second output signal; and

a fourth inverted amplifier circuit that receives the estimated common-mode output signal and a sum of the output signal of the second non-inverted amplifier and the output signal of the second inverted amplifier circuit, and outputs a third output signal and a fourth output signal,

wherein adding the second output signal and the fourth output signal creates the estimated common-mode output signal.

5. An operational amplifier circuit, comprising:

a first inverted amplifier circuit that receives a first input signal;

a second inverted amplifier circuit that receives a second input signal;

a non-inverted amplifier circuit that receives the first input signal and the second input signal and generates first and second common-mode input signals,

a third inverted amplifier circuit that receives an estimated

common-mode output signal and an added signal of the first common-mode input signal to an output signal of the first inverted amplifier circuit, and outputs a first output signal and a second output signal; and

a fourth inverted amplifier circuit that receives the estimated common-mode output signal and an added signal of a second common-mode input signal to an output signal of the second inverted amplifier circuit, and outputs a third output signal and a fourth output signal,

wherein adding the second output signal and the fourth output signal creates the estimated common-mode output signal.

6. The operational amplifier circuit according to claim 4, wherein the first and second input signals are differential input signals.

7. The operational amplifier circuit according to claim 4, further comprising:

a fifth inverted amplifier circuit that receives the output signal of the first inverted amplifier circuit and outputs an output signal fed back to the output of the first inverted amplifier circuit;

a sixth inverted amplifier that receives the output signal of the second inverted amplifier circuit and outputs an output signal fed back to the output of the second inverted amplifier circuit;

a seventh inverted amplifier circuit that receives the output signal of the first inverted amplifier circuit and outputs an output signal fed back to the output of the second inverted amplifier circuit; and

an eighth inverted amplifier that receives the output signal of the second inverted amplifier circuit and outputs an output signal fed back to the output of the first inverted amplifier circuit.

8. An operational amplifier circuit, comprising:

a first inverted amplifier circuit that receives a first input signal;

a second inverted amplifier circuit that receives a second input signal;

a third inverted amplifier circuit that receives an estimated common-mode output signal and an output signal of the first inverted amplifier circuit and outputs a first output signal and a second output signal;

a fourth inverted amplifier circuit that receives the estimated common-mode output signal and an output signal of the second inverted

amplifier circuit and outputs a third output signal and a fourth output signal; and

a non-inverted amplifier circuit that receives the first input signal and the second input signal and adds a signal proportional to the sum of the first and second input signals to each output signal of said first and second inverted amplifier circuits,

wherein adding the second output signal and the fourth output signal creates the estimated common-mode output signal.

9. The operational amplifier circuit according to claim 8, wherein the first and second input signals are differential input signals.

10. The operational amplifier circuit according to claim 8, further comprising:

a fifth inverted amplifier circuit that receives the output signal of the first inverted amplifier circuit and outputs an output signal fed back to the output of the first inverted amplifier circuit;

a sixth inverted amplifier circuit that receives the output signal of the second inverted amplifier circuit and outputs an output signal fed back to the output of the second inverted amplifier circuit;

a seventh inverted amplifier circuit that receives the output signal of the first inverted amplifier circuit and outputs an output signal fed back to the output of the second inverted amplifier circuit, and

an eighth inverted amplifier circuit that receives the output signal of the second inverted amplifier circuit and outputs an output signal fed back to the output of the first inverted amplifier circuit.

11. The operational amplifier circuit according to claim 8, further comprising:

a second non-inverted amplifier circuit that receives the estimated common-mode output signal and outputs an output signal fed back to the output of the first inverted amplifier circuit; and

a third non-inverted amplifier circuit that receives the estimated common-mode output signal and outputs an output signal fed back to the output of the second inverted amplifier circuit.

12. A sample/hold circuit comprised of an operational amplifier circuit according to claim 1 and a capacitor that selectively connected to the operational amplifier circuit.

13. A filter circuit comprised of a first stage integrator using

the operational amplifier circuit according to claim 1 and subsequent stage integrators.

14. The filter circuit according to claim 13, wherein the subsequent stage integrators comprise an operational amplifier circuit according to claim 4.